IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

FG SRC LLC, Plaintiff, v. XILINX, INC., Defendant.	C.A. No. 20-cv-601-LPS **JURY TRIAL DEMANDED**

DEFENDANT XILINX, INC.'S OPENING CLAIM CONSTRUCTION BRIEF

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Dated: October 26, 2021

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I. INTRODUCTION

U.S. Patent No. 9,153,311 (the "'311 patent") relates to a system and method that allegedly improves upon prior art computing systems that include reconfigurable logic devices coupled to DRAM memory. The patent discloses a data maintenance block to control the self-refresh functionality of DRAM memory while the reconfigurable logic device is being reconfigured. The bulk of the parties' disputes focus on whether the claims should be interpreted as written (consistent with the preferred embodiment and virtually the entire specification) or whether the scope should be twisted to try and manufacture a case for SRC. Plaintiff FG SRC, who only recently acquired the patent, simply disagrees with what the inventor chose to claim and now seeks to use claim construction to rewrite the claims. The Court should deny this request.

II. TECHNICAL BACKGROUND

The '311 patent is titled "[s]ystem and method for retaining [dynamic random access memory (DRAM)] data when reprogramming reconfigurable devices with DRAM memory controllers." The patent relates to a system and method for maintaining DRAM memory contents for a reconfigurable logic device while the device is being reconfigured. A reconfigurable logic device, like a field programmable gate array (FPGA), refers to a logic device that can be reconfigured to perform various different functions.

Reconfigurable logic devices are often paired with external memory devices such as DRAM memory to provide additional data storage capabilities. DRAM is a type of volatile memory that uses electrical charge to store its information. DRAMs are usually paired with a memory controller that refreshes the memory, but some DRAMs are capable of internally

refreshing themselves if given constant instructions to do so. This process is referred to as "self-refresh." During reconfiguration, however, the reconfigurable device may become unable to reliably maintain the refresh or self-refresh state of the DRAM. This could lead to data corruption, or worse, data loss.

The '311 patent purports to solve this issue by providing a data maintenance block that independently controls the self-refresh mode while the reconfigurable logic is reconfigured. That is, as claimed, the data maintenance block is "operative to provide stable input levels on [the DRAM's] self-refresh command inputs while said reconfigurable logic device is reconfigured." Ex. A ('311 Pat.) at Cl. 1.

III. DISPUTED CLAIM TERMS

A. Term 1: *"data maintenance block coupled to said reconfigurable logic device"/"data maintenance block coupled to said reconfigurable device"*

Xilinx's Construction	SRC's Construction
"a data maintenance block connected as a separate component to said reconfigurable logic device"	The terms "data maintenance block" and "coupled to said reconfigurable logic device" should be construed separately, particularly as Defendant's proposal does not provide a construction for "data maintenance block", and Plaintiff has previously proposed constructions for each of these terms. "a device, separate from the memory controller, which drives command inputs and is connected to the reconfigurable logic device, where said device can be part of said reconfigurable logic device or can be external to said reconfigurable logic device"

The claims recite a data maintenance block ***coupled to*** a reconfigurable logic device or a reconfigurable device. *See, e.g.*, Ex. A ('311 Pat.) at Cls. 1 and 11. Xilinx asks the Court to construe this term as written to simply require that there be two claimed components connected together. SRC, on the other hand, asks the court to essentially strike the claimed "coupled to" and replace it with "connected to or part of." On top of this, SRC seeks to add an ambiguous negative limitation "separate from the memory controller" that is not required by the specification and is

solely intended to try and avoid the prior art. Xilinx's proposal, that the data maintenance block and reconfigurable logic device are separate components connected together, is the only interpretation that makes sense in the context of the '311 patent, the intrinsic and extrinsic record, and the knowledge of a POSITA.

1. **The intrinsic record supports Xilinx's construction that the data maintenance block and reconfigurable logic device are separate components**

a. <u>The patent claims show that the data maintenance block and the reconfigurable logic device are separate components</u>

The '311 claims, specification, and figures are clear that the claimed data maintenance block and the reconfigurable logic device are separate components connected together. It is a well-established principle that "the claims [of the patent] themselves provide substantial guidance as to the meaning of particular claim terms." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*). Here, it is undisputed that the independent claims require the data maintenance block to be "coupled to" the reconfigurable logic device.

For example, the claims recite in pertinent part (emphasis added):

> Claim 1: . . . [A] data maintenance block ***coupled to*** said reconfigurable logic device and self-refresh command inputs of said DRAM memory, said data maintenance block operative to provide stable input levels on said self-refresh command inputs while said reconfigurable logic device is reconfigured
>
> Claim 11: [P]roviding a data maintenance block ***coupled to*** said reconfigurable device.

In addition to the claim terms at issue, "the context of the surrounding words of the claim" and "[o]ther claims of the patent in question, both asserted and unasserted, can also be valuable" in discerning the meaning of a particular claim term. *Id.* (internal citation omitted). Here, the claims use the term "coupled to" to refer to separately connected components. For example, claim 1 of the '311 patent states that the reconfigurable logic device has a memory controller "coupled to" selected input and outputs of said DRAM memory. No one disputes in this case that the

claimed reconfigurable logic device is separate from the DRAM memory, as shown in Figures 1 and 2. Similarly, claim 17 of the '311 patent states that the command decode portion is "coupled to" selected inputs of the DRAM memory. *See* Ex. A ('311 Pat.) at Cl. 17. The command decode portion is a subcomponent of the data maintenance block, which is also undisputedly separate from DRAM memory. *See id.* at Cl. 12. Moreover, the command decode portion is separate from the reconfigurable logic device as it "[receives] commands from said reconfigurable device and [returns] acknowledgment signals in response thereto." *See id.* at Cl. 12. Thus, the applicant used the term "coupled to" to refer to a connection between separate components on numerous occasional in the claims. SRC will undoubtedly point to dependent claims 9 and 15 as supporting their argument that "coupled to" is not limited to two items actually being coupled together. However, as discussed further below, claims 9 and 15 are invalid because a dependent claim cannot fall outside the scope of its independent claim and, thus, cannot change the meaning prescribed by the other claims, the specification, or the record.

b. <u>The patent specification and figures show that the data maintenance block and the reconfigurable logic device are separate components connected together</u>

The patent "specification is [also] always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here, the patent specification is uniform in its use of the term "coupled to" both in the claimed context and generally. First, with regard to the data maintenance block and the reconfigurable logic device, the patent recites that the "a data maintenance block coupled to the reconfigurable logic device." Ex. A ('311 Pat.) at 3:42–44. This coupling is illustrated in Figure 1 below where the data maintenance block (106) and the reconfigurable logic device (104) are separately connected components.

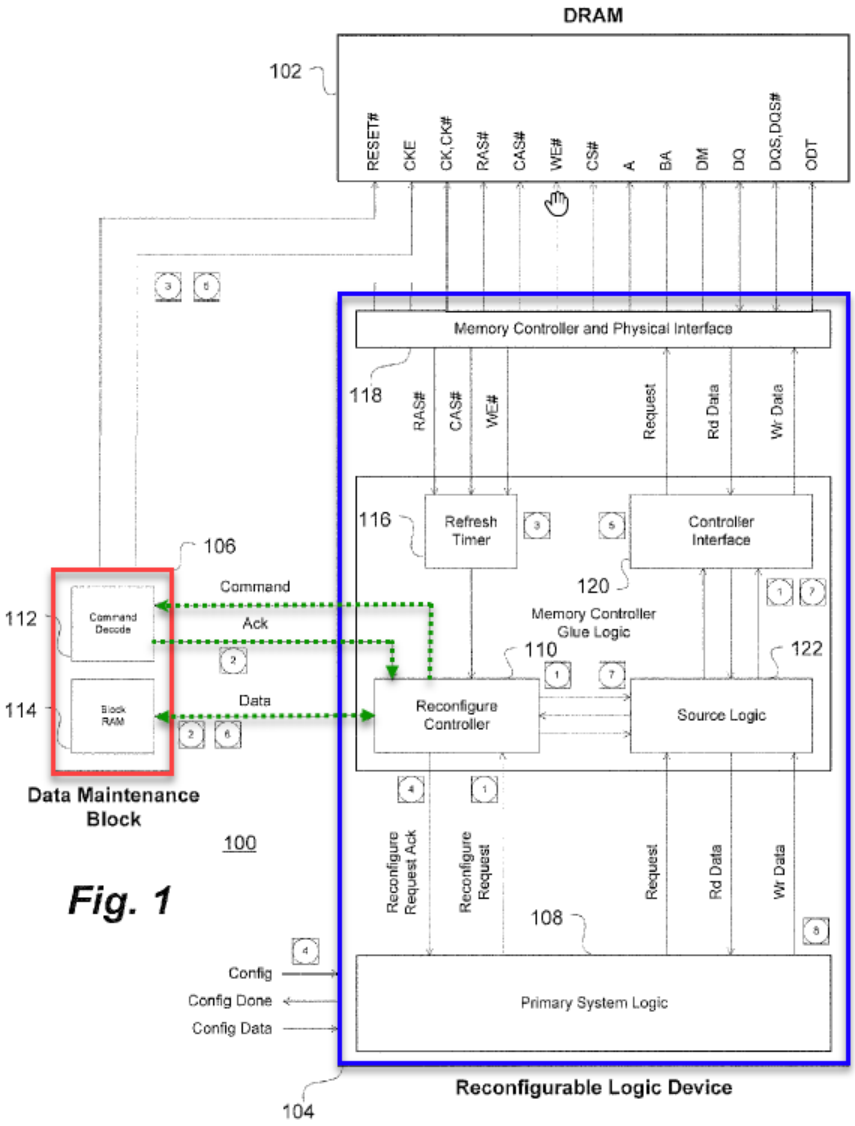

Fig. 1

See id. at Fig. 1. Figure 2 similarly illustrates the data maintenance block (106) separate from the reconfigurable application logic (202), and the patent explains that the "reconfigurable application logic 202 is coupled to the data maintenance blocks 106 and DRAM memory 102." *Id.* at Fig. 2 and 5:63–65. Indeed, the term "coupled to" is used 16 times in the '311 patent and always refers to a connection between two separate components. *See e.g., id.* at 6:1–2 ("The reconfigurable application logic 202 is also ***coupled to*** an SRC Computers, LLC SNAP™ and network processors block 206" referring to the connection between blocks 202 and 206; *see also id.* at 4:52–54 ("data

maintenance block 106 is coupled to the DRAM memory 102 to supply reset (RESET#) and clock enable (CKE#) signals" referring to the connection between the data maintenance block and the separate DRAM memory). The term "coupled to" is never used by the named inventors to refer to anything but a connection between two separate components.

As previously recognized by this Court, where a patent consistently uses the term "coupled to" to refer to separate components, the claim terms should be construed consistent with the patent. *See Wi-LAN Inc. v. Sharp Elecs. Corp.*, No. CV 15-379-LPS, 2018 WL 1997982, at *12 (D. Del. Apr. 27, 2018) ("The Court agrees with Defendants that the patent consistently uses 'coupled' to refer to components that are not sub-components of each other and 'in' to refer to components that could be sub-components of each other."). Much like the how the court in *Wi-LAN* identified the patentee's use of the term "in" to refer to subcomponents as "coupled" components, the '311 patent also uses the terms "in" or "portion of" to refer to subcomponents. *Id.*; *see also* Ex. A ('311 Pat.) at 4:37–39 ("A block RAM portion 114 of the data maintenance block 106"); *see also* Ex. A ('311 Pat.) at 3:7–9 ("another small section of block RAM 114 located in the data maintenance block 106"). The independent claims do not claim, however, that the data maintenance block is "in" or a "portion of" the reconfigurable logic device. *See e.g.*, Ex. A ('311 Pat.) at Cls. 1 and 11. The intrinsic record, therefore, supports Xilinx's construction that the data maintenance block and reconfigurable logic device are separately connected components.

c. The Prosecution History (and Equity) Support Xilinx's Construction[1]

Prior to the start of this case, Xilinx filed an IPR against the '311 patent. The PTAB expressly denied institution of that IPR because the prior art did not have a data maintenance block that was separate from and connected to the reconfigurable logic device. *See* Ex. B (IPR2018-

[1] PTAB decisions are part of the prosecution history. *See Nat'l Oilwell DHT, L.P. v. Amega W. Servs., LLC, No.* CV 2-14-1020, 2019 WL 1787250, at *8 (E.D. Tex. Apr. 24, 2019).

01395, Paper 17) at 20–25. In particular, the PTAB held that the "[s]pecification of the '311 patent recites the phrase 'coupled to' when referring to two distinct and separate elements that are connected to each other, consistent with the plain and ordinary meaning of this phrase." *See, e.g.*, *id.* at 23–24.

In reaching this conclusion, the PTAB specifically considered a prior art argument that would have placed the data maintenance block within the reconfigurable logic device (*i.e.*, the FPGA). The PTAB was not persuaded by this argument, because the combination would require "that the reconfigurable logic device be 'coupled to' itself," and "[s]uch an interpretation would be inconsistent with the use of the phrase 'coupled to' within the '311 patent." Ex. B (IPR2018-01395, Paper 17) at 23. The PTAB further noted that it reads "the embodiment in which data maintenance block 106 is provided as a portion of an FPGA to fall outside the scope of claim 1 precisely because claim 1 specifically refers to 'a data maintenance block *coupled to* said reconfigurable logic device.'" *Id.* at 24–25 (emphasis in original). The PTAB reconfirmed this position by denying reconsideration of its decision. Ex. C (IPR2018-01395, Paper 19).

While the PTAB's construction is not binding on this Court, their reasoning on the same patent and the same situation should be persuasive to this Court – especially where the PTAB decision is consistent with the specification and claims. Beyond this, principles of comity gravitate towards consistent decisions between Courts in the interest of fairness – especially where the parties are the same. Here, SRC asks this Court to let it have its cake and eat it too. It wants to avoid the prior art at the PTAB on one construction and yet be able to change the meaning of the claims to try and build an infringement case. It would be fundamentally unfair to Xilinx for it to be denied inexpensive resolution at the PTAB under one construction and yet then be subjected to litigation on the very construction that the PTAB denied.

2. The extrinsic record confirms that the data maintenance block must be separate from the reconfigurable logic device

The extrinsic evidence is consistent with the intrinsic record, and further confirms that the term "coupled to" signifies separate components. The district court may "look beyond the patent's intrinsic evidence and [] consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015).[2]

In view of the extrinsic evidence, a POSITA, at the time of the claimed invention, would have understood that the process of "coupling" requires connecting or joining separate components or circuitry. *See* Ex. D (The Authoritative Dictionary of IEEE Standard Terms (7th ed.)) at 247, "Coupling" ("(7) The association of two or more circuit or systems in such a way that power or signal information may be transferred from one system or circuit to another."); *see also* Ex. E (Wiley Electrical and Electronic Engineering Dictionary (2004)) at 151, "Couple" ("1. To join, link, or allow the transfer of energy. For instance, to join circuits. 2. That which has been joined, linked, or connected in a manner which allows the transfer of energy. For example, coupled circuits."); *see also Silicon Graphics, Inc. v. Nvidia Corp.*, 58 F. Supp. 2d 331 (D. Del. 1999) (noting that the patentee cited "a technical dictionary of electronics, which defines the term 'couple' as 'to connect two circuits so signals are transferred from one to the other.'); and Ex. F (Khatri Decl.) at ¶¶ 29–36.

[2] "Extrinsic evidence consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Markman*, 52 F.3d at 980. For instance, technical dictionaries can assist the court in determining the meaning of a term to those of skill in the relevant art because such dictionaries "endeavor to collect the accepted meanings of terms used in various fields of science and technology." *Phillips*, 415 F.3d at 1318. Expert testimony can also be useful "to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id.*

The extrinsic evidence supports Xilinx's construction that the data maintenance block and reconfigurable logic device would have been understood to be separately connected components.

3. SRC's construction defies the plain language, renders the claim inoperable, finds little support in the specification, and adds a vague unsupported negative limitation

First, as noted above, SRC's proposed construction is entirely inconsistent with the plain meaning of the word "coupled." In essence, SRC is seeking to redefine the word coupled to mean both "connected" and "be a part of." In theory, a patentee is free to act as its own lexicographer, but to do so, the patentee must "clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning." *See Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (quotation omitted). Here, the specification of the '311 patent nowhere suggests the term "coupled to" is intended to have any meaning other than what is customary, which is that "coupled to" refers to separately connected components.

Next, SRC's proposed construction would essentially render the claims inoperable.[3] Here, claim 1 requires that the data maintenance block "provide stable input levels on said [DRAM] self-refresh command inputs ***while said reconfigurable logic device is reconfigured***." SRC proposes a construction that would permit the data maintenance block to be part of the reconfigurable logic itself. A POSITA would have understood that while the reconfigurable logic device is being reconfigured, previously loaded configurations would be lost. Ex. F (Khatri Decl.) at ¶ 52. Thus, if the data maintenance block is "part of" the reconfigurable logic device, it would be erased when the logic device is reconfigured. *Id.* Put another way, one cannot both put the data maintenance

[3] "[W]here the claim language permits an operable construction, the inoperable construction is wrong." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 904 F.3d 965, 972 (Fed. Cir. 2018) (citing *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1345 (Fed. Cir. 2009)); *see also AIA Eng'g v. Magotteaux Int'l*, 657 F.3d 1264, 1278 (Fed. Cir. 2011) ("[A] construction that renders the claimed invention inoperable should be viewed with extreme skepticism.").

block within the programmable logic and simultaneously reconfigure that very logic where the data maintenance block is stored.[4] Such a configuration would cause "[i]ndeterminate states on the reset or clock enable inputs [which] results in DRAM data corruption," as explained in the specification of the '311 patent. *See* Ex. A ('311 Pat.) at 2:1–2.

Next, as noted above, there is little support in the specification for redefining "coupled to" to mean "connected to or part of," as SRC proposes. Xilinx does not deny that there are references in the specification to potential embodiments having an "internally located" data maintenance block, but the specification never provides a frame of reference for these statements – internal to the primary system logic 108, internal to the programmable logic device 104, or internal to the entire claimed system. Moreover, this potential "internal" embodiment is clearly not the preferred embodiment, is never described as changing the meaning of coupled, and is ***not the embodiment being claimed***. "'[A] claim need not cover all embodiments,' as a 'patentee may draft different claims to cover different embodiments.'" *FlatWorld Interactives LLC v. Samsung Elecs. Co.*, No. CV 12-804-LPS, 2014 WL 7464143, at *8 (D. Del. Dec. 31, 2014). Similarly, the two references in the specification to "partial reconfiguration" are bare references with no described connection to the data maintenance block at all. At best, they allude to an alternate unclaimed embodiment and cannot redefine this term.

Lastly, SRC's construction seeks to import a vague and unnecessary negative limitation - "separate from the memory controller." As an initial point, the properly construed claim language already makes it clear that the data maintenance block is separate from the *claimed* memory

[4] Notably, while Xilinx pioneered a technology that enables reconfiguration of only a portion of the reconfigurable logic, this technology is not recited in the claims of the '311 patent and the '311 patent provides no description (much less an enabling one) of how the data maintenance block could be located within a portion of the reconfigurable logic during a reconfiguration.

controller, because the claim requires that the memory controller be within the reconfigurable logic device, which is a separate component from the data maintenance block (as discussed above). It is only because SRC seeks to change the meaning of "coupled to" that it now feels compelled to introduce this new negative limitation. SRC realizes (correctly) that the specification describes having a "communication port…that allows the memory controller to direct self-refresh commands to the DRAM via the data maintenance block." Ex. A ('311 Pat.) at 2:17–20. In other words, the memory controller and the data maintenance block ***are coupled*** together via a communication port. While this is not an issue under the plain meaning, under SRC's view of "coupled to" this coupling would mean that the data maintenance block could be part of the recited memory controller (since they are also coupled together). Accordingly, SRC proposes a completely unnecessary negative limitation because while it wants the data maintenance block to be within the reconfigurable logic device, it does not want it to be part of the memory controller, which as the claims show is within the reconfigurable logic device. Accordingly, it again asks the Court to take a two-faced approach.

Beyond this, the proposed negative limitation is vague. Many devices have multiple memory controllers, and SRC is unclear if it is referring to the claimed memory controller or any memory controller within an Accused Product. As noted above, the claim language already makes it clear that the reconfigurable logic device (where the claimed memory controller resides) is separate from the data maintenance block. A negative construction is unnecessary and, indeed, only intended to try and "plug a hole" created by SRC's construction.

B. Term 2: *"coupled to said reconfigurable logic device"/"coupled to said reconfigurable device"*

Xilinx's Construction	**SRC's Construction**
"coupled to said reconfigurable logic device" (Claim 1) *"coupled to said reconfigurable device"* (Claim 11)	
"[a data maintenance block] connected as a separate component to said reconfigurable logic device"	"connected to the reconfigurable logic device, where the data

Xilinx's Construction	SRC's Construction
"coupled to said reconfigurable logic device" (Claim 1) *"coupled to said reconfigurable device"* (Claim 11)	
Xilinx contends that the term "coupled to said reconfigurable logic device" should not be construed independently.	maintenance block can be part of said reconfigurable logic device, or can be external to said reconfigurable logic device"

As discussed for Term 1 above, the claims recite a data maintenance block coupled to a reconfigurable logic device or a reconfigurable device. *See, e.g.*, Ex. A '311 Pat. at Cls. 1 and 11. SRC argues that the terms "data maintenance block" and "coupled to said reconfigurable logic device" should be separately construed. Xilinx disagrees as this division removes essential context and because the term "coupled to said reconfigurable logic device" is not used outside the context of a data maintenance block. For this term, SRC put forth a construction similar to its proposal for "a data maintenance block coupled to a reconfigurable logic device," as discussed for Term 1 above. SRC's construction of Term 2 is wrong for the same reasons.

C. Term 3: *"said reconfigurable logic device comprises said data maintenance block"/"providing a portion of said reconfigurable device as said data maintenance block"*

Xilinx's Construction	SRC's Construction
"said reconfigurable logic device comprises said data maintenance block" (Claim 9) *"providing a portion of said reconfigurable device as said data maintenance block"* (Claim 15)	
Indefinite under 35 U.S.C. § 112.	The term is not indefinite and has its plain and ordinary meaning; no construction is required.

Dependent claims 9 and 15 respectively recite "said reconfigurable logic device comprises said data maintenance block" and "providing a portion of said reconfigurable device as said data maintenance block." *See, e.g.*, Ex. A ('311 Pat.) at Cls. 9 and 15. The dispute for this term turns on whether the claim language is indefinite. SRC argues that these dependent claims are not indefinite and subject to their plain and ordinary meaning. However, dependent claims 9 and 15

are outside the scope of their respective independent claims, so these claims fail to establish the scope of the claimed invention with reasonable certainty.

As an initial point, in denying institution, the PTAB has essentially already found that claim 9 was outside the scope of independent claim 1. In particular, the PTAB held that an "embodiment in which data maintenance block 106 is provided as a portion of an FPGA [falls] ***outside the scope of claim 1*** precisely because claim 1 specifically refers to 'a data maintenance block ***coupled to*** said reconfigurable logic device.'" Ex. B (IPR2018-01395, Paper 17) at 24–25. The embodiment which the PTAB found outside the scope of claim 1 was precisely claim 9. While claim 15 was not before the Board, its scope matches claim 9.

Like the PTAB, upon reading dependent claims 9 and 15, a POSITA would not have understood the scope of the claimed invention. It is a logical impossibility. A patent claim is indefinite if, "viewed in light of the specification and prosecution history, [it fails to] inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). For dependent claims, it is "axiomatic that a dependent claim cannot be broader than the claim from which it depends." *Dow Chem. Co. v. United States*, 226 F.3d 1334, 1341-42 (Fed. Cir. 2000); *see also Uni-Systems, LLC v. U.S. Tennis Ass'n Nat'l Tennis Ctr. Inc.*, No. 17-CV-147(KAM)(CLP), 2020 U.S. Dist. LEXIS 122699, at *86–87 (E.D.N.Y. July 13, 2020) (finding the term "very small side load" indefinite because it was broader than its respective independent claim).

The use of the terms "reconfigurable logic device" and "data maintenance block" in independent claims 1 and 11 is wholly inconsistent with how the terms are subsequently used in dependent claims 9 and 15, rendering them indefinite. In particular, the independent claims require that the data maintenance block and the reconfigurable logic device be coupled together whereas

dependent claims 9 and 15 permit the data maintenance block to be part of the reconfigurable logic device such that the device would no longer be coupled to the data maintenance block. Or as the PTAB put it, the reconfigurable logic device cannot be coupled to itself. Ex. B (IPR2018-01395, Paper 17) at 23.

While this fact is self-evident from the inconsistent language of the claims, a POSITA reading the claims would have seen it as a fundamental disconnect and impossibility that the data maintenance block could be both ***coupled to*** the reconfigurable logic device, as required by independent claims 1 and 11, and also be ***part of*** the reconfigurable logic device, as required by claims 9 and 15. Ex. F (Khatri Decl.) at ¶¶ 40–55. This is especially significant here as under the scope of claims 1 and 11, the data maintenance block is outside the reconfigurable portion (and thus not made from reconfigurable logic) whereas claims 9 and 15 require the opposite. *Id. at* ¶ 42–45.

D. Term 4: *"data maintenance block"*

Xilinx's Construction	SRC's Construction
"data maintenance block" (Claims 1, 4, 5, 6, 9, 10, 11, 12, 13, 15, 17, 19)	
"a unit of circuitry separate from the reconfigurable logic device that drives refresh command inputs"	"a device, separate from the memory controller, which drives self-refresh command inputs"

Several claims recite a "data maintenance block." *See, e.g.*, Ex. A ('311 Pat.) at Cls. 1 and 11. The parties do not dispute that the data maintenance drives self-refresh command inputs.[5] The

[5] The patent's claims and specification demonstrate that a data maintenance block is a unit of circuitry that drives self-refresh command inputs. For example, claim 1 of the '311 patent states that the "data maintenance block [is] coupled to . . . self-refresh command inputs of said DRAM memory [and] operative to provide stable input levels on said self-refresh command inputs while said reconfigurable logic device is reconfigured." *See* '311 Patent at Cl. 1. The patent specification further states that "the data maintenance block 106 may be conveniently provided as a complex programmable logic device (CPLD) or other separate integrated circuit device," consistent with Xilinx's proposed construction. *See* '311 Patent at 4:23–29.

primary dispute for this term is whether the data maintenance block is separate from the reconfigurable logic device, as discussed above. In this regard, the parties' constructions for this term rely on the same arguments as those of Terms 1 and 2. Xilinx's construction for "data maintenance block" is correct for the same reasons, and "stays true to the claim language and most naturally aligns with the patent's description of the invention," and is therefore "the correct construction." *Renishaw*, 158 F.3d at 1250. SRC's construction also seeks to add the language "separate from the memory controller." This addition is improper and is addressed below with regard to the term "memory controller," for which SRC proposes the reciprocal requirement.

E. Term 5: *"command decode portion"*

Xilinx's Construction	SRC's Construction
"command decode portion" (Claims 4, 5, 12, 17)	
"a block of circuitry that translates commands to perform specific functions"	Plain and ordinary meaning; no construction is required.

The command decode portion is a subcomponent of the data maintenance block. The intrinsic record, therefore, supports that the command decode portion is "a block of circuitry" for the same reasons discussed above with regard to the "data maintenance block." *See* Term 4 ("data maintenance block"). Moreover, the patent's claims and specification demonstrate that the command decode portion translates commands to perform specific functions. For example, claim 12 of the '311 patent states that the "command decode portion [receives] commands from said reconfigurable device and [returns] acknowledgment signals in response thereto." *See* Ex. A ('311 Pat.) at Cl. 12. The patent specification makes clear that the data maintenance block may perform specific functions in response to the command such as storing data in block RAM. *See id.* at 4:34–39, 5:7–12.

F. Term 6: *"memory controller"*

Xilinx's Construction	SRC's Construction
"memory controller" (Claims 1 and 11)	
"non-configurable circuitry that controls the operation of the memory, and is coupled to DRAM inputs and outputs where the data maintenance block is not connected"	"reconfigurable integrated circuit—within the part of the reconfigurable logic device that is to be reconfigured—operable to manage the flow of data to and from DRAM"

Xilinx's proposed construction defines "memory controller" consistent with the patent claims and specification. SRC's proposed construction seeks to introduce multiple requirements that conflict with the preferred embodiment in the patent. First, as to the language itself, independent claim 1 states that the memory controller is "coupled to selected inputs and outputs of said DRAM memory." The language is notable, because it shows that the memory controller is coupled to certain, but not all, of the inputs and outputs.

This claim language flows directly from the specification which consistently and repeatedly confirms that the claimed memory controller is defined by being coupled to the DRAM inputs and outputs to which the data maintenance block is not coupled. For example, in the Summary of the Invention section of the patent, the patentee explains that the memory controller is "coupled to selected inputs and outputs of the DRAM memory and a data maintenance block coupled to the reconfigurable logic device and self-refresh command inputs of the DRAM memory." Ex. A ('311 Pat.) at 3:31–36. Further, in describing the invention, the patentee explains that the memory controller and the data maintenance block are coupled to mutually exclusive DRAM input and outputs. *See id.* at 4:42–54 (describing that the memory controller is connected to variety of specific signals but not the RESET# and CKE# signals that are connected to the data maintenance block." This division of connection is also illustrated in Figure 1 below:

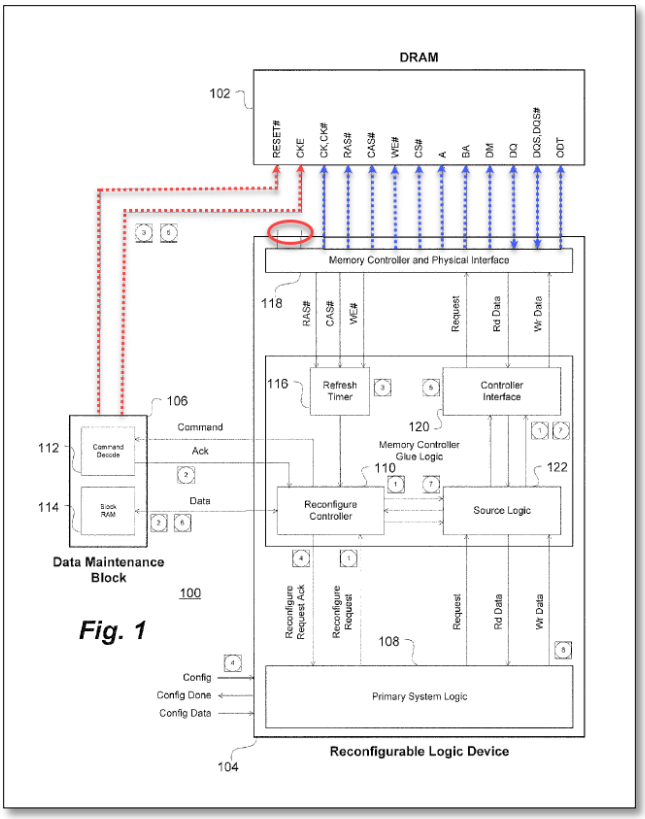

Fig. 1

As shown above, the memory controller is coupled to one set of inputs/outputs and the data maintenance block to another (the self-refresh inputs). Figure 1 even illustrates that the memory controller is ***expressly not coupled*** to self-refresh command inputs (the red circle above). This is because the inventors shifted that functionality to the data maintenance block, as also confirmed by the Abstract, which explains that "[t]he DRAM memory controller is utilized in concert with ….[a] data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/0) and the data maintenance block drives the self-refresh command inputs" *id.* at 6–8; *see also id.* at 2:17–20 (explaining that self-refresh commands are sent via the data maintenance block, which alone is connected to the DRAM memory: "a communication port is implemented between the FPGA and the data maintenance block that allows the memory controller in the FPGA to direct the self-refresh 20 commands to the DRAM via the data maintenance block.").

Beyond this, SRC's proposed construction is fundamentally at odds with the teachings of the '311 patent. In particular, SRC seeks to inject requirements that the memory controller be both (a) a reconfigurable integrated circuit, and (b) within the part of the reconfigurable logic device that is to be reconfigured. These requirements, which are meant to try and avoid the prior art, find no support in the claims or specification, and, as set forth in Xilinx's proposed construction are the literal opposite of what is described in the '311 patent.

While the claimed memory controller must be on the reconfigurable logic device, ***it is not reconfigurable itself***. Indeed, as shown in Figure 1 above, the reconfigurable part of the reconfigurable logic device is the Primary System Logic 108. The Memory Controller Glue Logic (elements 110, 116, 120, and 122) as well as the memory controller itself and physical interface (element 118) are supporting circuitry that are never described as being reconfigurable. Indeed, as shown in Figure 1 above, only the Primary System Logic 108 has reconfiguration inputs and is described in the patent as being reconfigurable. *See* Ex. A ('311 Pat.) at 5:17–26 (describing reconfiguration in connection with numerals 4 and 5 from Figure 1). While the '311 patent makes reference to reconfiguration numerous times, it never once describes reconfiguring the memory controller, and Figure 1 ***shows no connection between the reconfiguration controller and the memory controller*** nor any other mechanism to reconfigure the memory controller 118.[6]

G. <u>Terms 7 and 8</u>: *"received from" and "returning said data to"*

Xilinx's Construction	**SRC's Construction**
"received from" (Claims 7, 11, 13, 17)	

[6] To the extent that the Court finds that the memory controller must be reconfigurable because it resides on a device called a "reconfigurable logic device," Xilinx requests that the Court apply this same logic to the claimed reconfiguration controller, as it similarly resides on the reconfigurable logic device. While Xilinx has agreed to a meaning for reconfiguration controller with SRC, this agreement was predicated on the understanding that the supporting circuitry on the reconfigurable logic device was not reconfigurable.

Xilinx's Construction	SRC's Construction
"accepted from a separate component"	Plain and ordinary meaning; no construction is required.
"returning said data to" (Claim 13)	
"restoring data to a separate component after prior receipt therefrom"	Plain and ordinary meaning; no construction is required.

The primary dispute for these claim terms is whether the terms have a plain and ordinary meaning (as SRC contends) or denote a relationship between two separate components (as Xilinx proposes). A determination that a claim term has "plain and ordinary meaning" may be inadequate "when reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech*. Co., 521 F.3d 1351, 1361 (Fed. Cir. 2008). Claim construction is therefore required in this instance.

The claims only use the precise phrase "received from" in relation to an exchange between the data maintenance block and the reconfigurable logic device, which Xilinx contends are separate as discussed above. The term "returning said data to" is used in a similar manner. It follows that, in the context of the claimed invention, the terms "received from" and "returning said data to" can only refer to exchanging data with a separate component, as proposed by Xilinx. Xilinx's constructions, therefore, both address the dispute between the parties and further "align[] with the patent's description of the invention." *Renishaw*, 158 F.3d at 1250. Moreover, both the intrinsic and extrinsic evidence support Xilinx's proposed constructions. The patent persistently uses these claim terms when referring to separately connected components. For example, Claim 14 of the '311 patent states that the data maintenance block receives data from, and returns data to, DRAM memory, in which the data maintenance block and DRAM memory are indisputably separate components. *See* Ex. A ('311 Pat.) at Cl. 1; *see also* Ex. F (Khatri Decl.) at ¶ 33.

Furthermore, a POSITA would have understood that "receive" and "return" respectively refer to "accept" and "restore," in the claimed invention. *See, e.g.*, Ex. G (Dictionary of Computing

(6th ed.)) at 279, "receive" ("to accept data from a communications link"); *see also* Ex. E (Wiley Electrical and Electronic Engineering Dictionary (2004)) at 660, "restore" ("to reset or otherwise go back to a former condition; to return computer data to the state it was in before an error or failure").

H. Term 9: *"A computer system comprising"*

Xilinx's Construction	SRC's Construction
"A computer system comprising" (Claim 1)	
The preamble is limiting.	The preamble is not limiting.

The parties dispute whether the term "[a] computer system comprising" is limiting preamble language. Xilinx contends that it is. "In general, a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). While no litmus test defines when a preamble limits claim scope, one guidepost is whether the preamble recites structure underscored as important by the specification. *Id.*

Here, the specification makes clear that the computing system is of paramount importance to the claim invention. Indeed, the claimed invention would fail to exist without it. Inasmuch, the disputed term, or other variations thereof, is used prominently throughout the specification, demonstrating that the inventors intended it to be a central aspect of the invention. *See* Ex. A ('311 Pat.) at 1:5–15, 3:5–10, 3:25–30, 3:30–40, 3:59–64, 4:5–14; *see also Poly–Am., LP v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004) (finding that a preamble was limiting because, in addition to the fact that the preamble was related to structural features, the preamble term was repeated throughout the patent specification, e.g., in the title and summary of the invention.).

IV. CONCLUSION

Xilinx respectfully requests the Court adopt its proposed constructions.

Dated: October 26, 2021

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